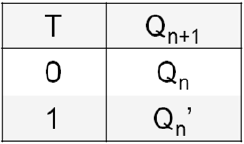
WRES1102/WIC2003

1. Create a VHDL design for a T Flip-Flop using IF statement (e.g. Tflip.vhd). Then create a test bench that able to test your design. Your top level design should contain Reset, T, Clock, Q and Q\_bar. The output Q will produce ‘0’ when Reset is ‘1’. The behavior of the T Flip-Flop is as below



1. From the T Flip-Flop, write VHDL code for a 4-bit asynchronous counter without using generate statement (e.g. asynCtr.vhd). Write another VHDL code for an n-bit asynchronous counter using generic and generate statement (e.g. asynCtrGEN.vhd). Write a testbench (e.g asynCtrTB.vhd) that will display the following output. Use also assert statement to ensure that both asynCtr.vhd and asynCtrGEN has the same output.

